

REMARKS/ARGUMENTS

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this Application in view of the following remarks.

The Applicants originally submitted Claims 1-42 in the application. In previous responses, the Applicants cancelled Claims 8 and 18 without prejudice or disclaimer, and submitted Claims 43-44 for examination. Accordingly, Claims 1-7, 9-17 and 19-44 are currently pending in the Application.

I. Formal Matters

The Applicants note with appreciation that the Examiner has indicated that Claims 21-42 are in condition for allowance.

II. Rejection of Claims 1-7, 9-17, 19, 20, 43 and 44 under 35 U.S.C. § 102(e)

The Examiner has rejected Claims 1-7, 9-17, 19, 20, 43 and 44 under 35 U.S.C. § 102(e) as being unpatentable over U.S. Patent No. 6,807,581 to Starr, *et al* ("Starr"). The Applicants respectfully traverse the rejection, because Starr fails to teach each and every element of the claims.

Claims 1 and 11 include the limitation "an array of arithmetic logic units." The Examiner asserts that FIG. 17C and col. 24, lines 6-8 of Starr anticipate "a plurality [of] arithmetic logic units." The Applicants respectfully state that the cited portions of Starr fail to disclose an "*array of arithmetic logic units*." Column 24, lines 5-8 of Starr state: "FIG. 17C depicts the third microprocessor phase 900, which includes ALU and queue operations. The ALU 902 includes an

adder, priority encoders and other standard logic functions. Results of the ALU are stored in registers ALU output 918, ALU condition codes 920 and destination operation results 922.”

A single ALU may be disclosed in the above-cited passage of Starr, the ALU having “an adder, priority encoders and other standard logic functions.” However, the Applicants respectfully state that, although the above passage may disclose a single ALU, there is no disclosure of an *array of arithmetic logic units* as is claimed in independent Claims 1 and 11.

Furthermore, in FIG. 17C of Starr, referenced in the above-cited passage of Starr, only a single ALU 902 is disclosed. ALU output 918 and ALU CCS 920, both of which are coupled to ALU 902, are registers: register ALU output 918 and registers ALU condition codes 920. These may be registers for employment with ALU 902, but they are not the array of arithmetic logic units as claimed in independent Claims 1 and 11.

Therefore, Starr does not anticipate the element “a programmable logic core having an array of arithmetic logic units...” as claimed in independent Claims 1 and 11, and therefore does not defeat the novelty of independent Claims 1 and 11. Thus, Claims 1 and 11, and those claims depending therefrom, are allowable. Accordingly, the Applicants respectfully request that the Examiner withdraw the rejection of 1-7, 9-17, 19, 20, 43 and 44 under 35 U.S.C. § 102(e) and allow issuance thereof.

III. Conclusion

In view of the foregoing remarks, the Applicants now see all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for all of the pending Claims, including Claims 1-7 and 9-44.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present Application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 12-2252.

Respectfully submitted,

HITT GAINES, PC

A handwritten signature in cursive script, appearing to read "J. Joel Justiss".

J. Joel Justiss

Registration No. 48,981

Dated: February 8, 2007

P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800